Hossein Karimiyan Alidash

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Education:

Post-Doc Research Fellowship, Polytechnic of Turin
Research Area: "**Process Variation and NBTI Aging Sensor Circuit Design**"
February 2011 – January 2012, Polytechnic of Turin, Italy.

Ph. D. in Electrical Engineering,
Research Area: "**Low-Power Digital Design - State Retention Clocked Storage Elements**"
September 2003 – July 2010, Isfahan University of Technology, Isfahan, Iran.

M.Sc. in Electronics Engineering
From September 1998 to February 2001, Isfahan University of Technology, Isfahan, Iran.
M.Sc. Thesis title: "***Application of Fuzzy Controller on DC-DC Converters***"

B.Sc. in Electronics Engineering,
From September 1992 to July 1997, Urmia University, Urmia, Iran.

Research Interests:

- Low-Power Digital Design
- Hardware Description/Verification Language: Verilog / System Verilog
- Implementation of Digital Signal Processing Blocks on FPGA
- Low-Voltage High-Current Power Supply Circuit
- Data Converter Design, ADC, DAC, and TDC
- ASIC Prototyping on Programmable Logic Device
- IP Design and Verification
- High Speed Digital PCB Design
- High Speed Computer Networking

Publication:

Book:

H.Karimiyan, F.Heidari, **Digital System Design Using Verilog HDL**, CSP Tehran, 2002.

Journal Papers:

1) Hossein Karimiyan, Andrea Calimera, Alberto Macii, Enrico Macii, and Massimo Poncino, “An on-chip all-digital PV-monitoring architecture for digital IPs,” Proceedings of the 21st international conference on Integrated circuit and system design: power and timing modeling, optimization, and simulation (PATMOS'11), pp. 162-172.
2) Hossein Karimiyan Alidash, Sayed Masoud Sayedi, “Activity aware clock gated storage element design,” 19th Iranian Conference on Electrical Engineering (ICEE), 2011, pp.1-4, 17-19 May 2011.
3) H. Karimiyan, M. Sayedi, and H. Saidi, “Low-Power Dual-Edge Triggered State Retention Scan Flip-Flop,” IET Computer and Digital Techniques, Vol. 4, Issue 5, pp. 410-419, Sept. 2010.
4) H. Karimiyan Alidash, M. Sayedi, and H. Saidi, “Low-Power State Retention Pulsed Latch,” 18th Iranian Conference on Electrical Engineering (ICEE), pp. 417-420, Isfahan, 2010.
5) H. Karimiyan Alidash and Vojin G. Oklobdzija., “Low-Power Soft Error Hardened Latch,” J. Low Power Electron. Vol. 6, pp. 218-226 (2010).

Conference Papers

۱) زهرا خجسته و حسین کریمیان علیداش، " طراحی و بهینه سازی حسگر اندازه گیری تمام دیجیتال تغییرات فرآیند ساخت و سالمندی"، بیست و چهارمین کنفرانس ملی سالانه انجمن کامپیوتر ایران، ۱۳۹۷.

۲) علیرضا قمی و حسین کریمیان علیداش، " طراحی حسگرتصویر هوشمند جهت پیادهسازی سختافزاری فیلترهای پردازش تصاویر مناسب برای کاربردهای اینترنت اشیا،"، بیست و چهارمین کنفرانس ملی سالانه انجمن کامپیوتر ایران، ۱۳۹۷.

3) Alidash, Hossein Karimiyan, Andrea Calimera, Alberto Macii, Enrico Macii, and Massimo Poncino. "On-Chip NBTI and PBTI Tracking through an All-Digital Aging Monitor Architecture." In *International Workshop on Power and Timing Modeling, Optimization and Simulation*, pp. 155-165. Springer, Berlin, Heidelberg, 2012.

٤) علی اصغر سعادت زاده و حسین کریمیان علیداش، " لچ استاتیک مقاوم در برابر خطای نرم با تأخیر و توان مصرفی پایین"، بیستمین کنفرانس ملی سالانه انجمن کامپیوتر ایران، ۱۳۹۳.

٥) حسین کریمیان علیداش، " طراحی، تحلیل و ساخت برد پردازنده مرکزی با قابلیت اطمینان بالا"، دومین کنفرانس ملی اویونیک ایران، دانشگاه صنعتی اصفهان، ۱۳۹۳.

٦) حسین کریمیان علیداش و علی اصغر سعادت زاده، " قابلیت اطمینان سامانه های هوافضای دیجیتال در برابر برخورد ذرات پرانرژی اتمی "، دومین کنفرانس ملی اویونیک ایران، دانشگاه صنعتی اصفهان، ۱۳۹۳.

۷) حسین کریمیان علیداش، " طراحی، تحلیل، ساخت و تست برد مدار واسط سامانه ناوبری با قابلیت خودآزمونی "، کنفرانس بین المللی ناوبری ، دانشگاه صنعتی شریف، ۱۳۹۵.

8) H. Karimiyan Alidash, M. Sayedi, and H. Saidi, “Low-Power State Retention Pulsed Latch,” 18th Iranian Conference on Electrical Engineering (ICEE), pp. 417-420, Isfahan, 2010.
9) D., Baran, M., Aktan, H., Karimiyan, V.G., Oklobdzija, “Switching activity calculation of VLSI adders,” ASICON '09. IEEE 8th International Conference on ASIC, pp. 46-49, 2009.
10) H.K., Alidash, S.M., Sayedi, H., Saidi, V.G., Oklobdzija, “Soft error filtered and hardened latch,” ASICON '09. IEEE 8th International Conference on ASIC, pp. 613-616, 2009.
11) H. Karimiyan, M. Sayedi, and H. Saidi, “Low-Power Dual-Edge Triggered State Retention Scan Flip-Flop,” PATMOS2009, Integrated Circuit and System Design, Power and Timing Modeling, Optimization and Simulation, pp. 156-164, Delft, Netherlands.
12) H. Karimiyan Alidash and Vojin G. Oklobdzija., “Low-Power Soft Error Hardened Latch,” PATMOS2009, Integrated Circuit and System Design, Power and Timing Modeling, Optimization and Simulation, pp. 256-265, Delft, Netherlands.
13) Baran, D., Aktan, M., Karimiyan, H., Oklobdzija, V.G., “Exploration of switching activity behavior of addition algorithms,” MWSCAS '09. 52nd IEEE International Midwest Symposium on Circuits and Systems, pp. 523-526, 2-5 Aug. 2009.
14) H. Karimiyan, M. Sayedi, and H. Saidi, “Low-Power Dual Edge Triggered Level Converter Free Flip-Flop,” 16th Iranian Conference on Electrical Engineering (ICEE), pp. 399-404, May13-15, Tehran, 2008.
15) H. Karimiyan, M. Sayedi, and H. Saidi, “Low-Power Low-Leakage Static Flip-Flop,” 16th Iranian Conference on Electrical Engineering (ICEE), pp. 405-410, May13-15, Tehran, 2008

Teaching Experiences:

- Data Converter, University of Kashan
- VLSI Design, University of Kashan
- Advanced Digital Design, University of Kashan
- Digital Design, University of Kashan
- Computer Architecture, University of Kashan
- Microprocessor System Design, University of Kashan
- Electronic-I, University of Kashan
- Electronic-II, University of Kashan
- Electronic-III, University of Kashan
- Solid State Pulse Techniques , University of Kashan
- Digital Design Using FPGA and Verilog-HDL, Isfahan University of Technology

Supervised Thesis

- Design of voltage to time converter suitable for time to digital converters
- Optimizing Fractals Key Generation Using DSP48 Blocks on FPGA Architecture
- Design of storage element suitable for time-to-digital converters
- Design of Soft Error Resilient Sequential Elements in Digital Circuits
- Digital Error Correction for Pipeline Analog to Digital Converter
- Design and Optimization of Sampling Circuit in Low-Voltage Data Conversion Systems
- Design & Optimization of APS Cell in Low Power, Low Voltage Image Sensors
- Design and Optimization of Graphene based Scannable D-Flip-Flop
- Design of Vernier Time to Digital Converter With Tunable Resolution
- Implementation & Optimization of CORDIC Algorithm Using DSP48 Hardware Multiplier Block
- Design and Optimization of All Digital Process Variation and Aging Measurement Sensor
- Design and Simulation of Image Sensor Based on 2D Material and Comparison with the improved Geometry Detector
- Design and Optimization of I/O Block Based on Graphene Nano-Ribbon FETs (GNRFETs)
- Design of readout circuit for smart image sensor with the aim of hardware-level implementation of image processing filters

Projects

- Smart Image Sensor Design for IOT Application
- Cosmic Ray and Neutron Hit Effect on Electronics Integrated Circuit and Hardening Methods
- Study, design, and fabrication of SBC
- Study, design, and fabrication of Interface
- Design, implantation and test of submergible robotic system